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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
FENNEMA, ROBERT E	
ART UNIT	**PAPER NUMBER**
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/781,883	SEAL ET AL.	
	Examiner	Art Unit	
	Robert E. Fennema	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-33 have been considered. Claims 1, 12, and 23 amended as per Applicant's request.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 1 indicates that the instruction decoder is simultaneously configured in both a first and a second mode, which is not something that one of ordinary skill in the art would be capable of using without undue experimentation, since the entire point of modes is that you choose one or the other, not both. For the purposes of examination, Examiner is interpreting the claim language to be that the decoder can be configured in either a first or a second mode, which is consistent with the limitations in the other independent claims.

5. Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 1 indicates that the instruction decoder is simultaneously configured in both a first and a second mode, and the Applicant does not appear to have support for this limitation in their specification.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 1 indicates that the instruction decoder is configured in both a first and second mode at the same time, which is impossible, as it defies the definition of what a mode is, therefore it is not clear if the Applicant is attempting to claim one mode, or two modes, and if the decoder actually is switching between these modes or not.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-6, 8-17, 19-28, and 30-33 are rejected under 35 U.S.C. 102(e) as being anticipated by Qureshi et al. (United States Patent Application Publication 2004/00308856, herein Qureshi).

10. As per Claim 1, Qureshi teaches: An apparatus for processing data, said apparatus comprising:

data processing logic configured to perform data processing operations (Paragraph 13, this is what processors do); and

an instruction decoder configured to decode program instructions specifying data processing operations to be performed by said data processing logic and to control said data processing logic to perform said data processing operations (Paragraph 5, the decode logic); wherein

said instruction decoder is configured in a first mode in which program instructions of a first instruction set are decoded (Paragraph 5, little endian) and in a second mode in which program instructions of a second instruction set are decoded (Paragraph 5, big endian), a subset of program instructions of said first instruction set having a common storage order compensated encoding with a subset of program instructions of said second instruction set such that, after compensating for storage order differences, all bits are identical (See Tables 1 and 2 on pages 1 and 2

respectively) and forming a common subset of instructions representing at least one class of instructions (Paragraphs 14 and 16, the instructions are the same, just stored differently), said common subset of instructions controlling said data processing logic to perform the same data processing operations independent of whether said instruction decoder is operating in said first mode or said second mode (Paragraphs 14 and 16, the instructions are the same, just stored differently).

11. As per Claim 12, Qureshi teaches: A method of processing data, said method comprising the steps of:

performing data processing operations with data processing logic (Paragraph 13, this is what processors do); and

decoding with an instruction decoder program instructions specifying data processing operations to be performed by said data processing logic and controlling said data processing logic to perform said data processing operations (Paragraph 5, the decode logic); wherein

in a first mode program instructions of a first instruction set are decoded (Paragraph 5, little endian) and in a second mode program instructions of a second instruction set are decoded (Paragraph 5, big endian), a subset of program instructions of said first instruction set having a common bit-length and a common storage order compensated encoding with a subset of program instructions of said second instruction set such that, after compensating for storage order differences, all bits are identical (See Tables 1 and 2 on pages 1 and 2 respectively) and forming a common subset of

instructions representing at least one class of instructions (Paragraphs 14 and 16, the instructions are the same, just stored differently), said common subset of instructions controlling said data processing logic to perform the same data processing operations independent of whether said instruction decoder is operating in said first mode or said second mode (Paragraphs 14 and 16, the instructions are the same, just stored differently).

12. As per Claim 23, Qureshi teaches: A computer program product having a computer program operable to control a data processing apparatus containing data processing logic operable to perform data processing operations (Paragraph 13, this is what processors do), said computer program comprising:

program instructions of a first instruction set (Paragraph 5, little endian) and program instructions of a second instruction set (Paragraph 5, big endian), that control said data processing logic to perform said data processing operations;

wherein a subset of program instructions of said first instruction set have a common bit-length and a common storage order compensated encoding with a subset of program instructions of said second instruction set such that, after compensating for storage order differences, all bits are identical (See Tables 1 and 2 on pages 1 and 2 respectively) and form a common subset of instructions representing at least one class of instructions (Paragraphs 14 and 16, the instructions are the same, just stored differently), said common subset of instructions controlling data processing logic to perform the same data processing operations independent of whether instructions of

said first instruction set or of said second instruction set are being decoded (Paragraphs 14 and 16, the instructions are the same, just stored differently).

13. As per Claim 2, Qureshi teaches: The apparatus as claimed in claim 1, wherein said instruction decoder is operable to use common portions of said data processing logic to execute instructions of said common subset of instructions (Column 5, there is only one set of logic, which works regardless of the mode).

Claims 13 and 24 are substantially similar to Claim 2, and are rejected for the same reasons.

14. As per Claim 3, Qureshi teaches: The apparatus as claimed in claim 1, wherein said common subset of instructions includes a class of instructions being coprocessor instructions operable to control coprocessor data processing operations using coprocessor logic common to said first instruction set and said second instruction set (Column 5, there is only one set of logic, which works regardless of the mode).

Claims 14 and 25 are substantially similar to Claim 3, and are rejected for the same reasons.

15. As per Claim 4, Qureshi teaches: The apparatus as claimed in claim 3, wherein all unconditional coprocessor instructions are within said common subset (Column 5, all instructions are in the subset).

Claims 15 and 26 are substantially similar to Claim 4, and are rejected for the same reasons.

16. As per Claim 5, Qureshi teaches: The apparatus as claimed in claim 1, wherein said first instruction set is a fixed length instruction set of N-bit instructions (Column 21).

Claims 16 and 27 are substantially similar to Claim 5, and are rejected for the same reasons.

17. As per Claim 6, Qureshi teaches: The apparatus as claimed in claim 5, wherein N is one of 32 or 16 (Column 21, it is 32 bits).

Claims 17 and 28 are substantially similar to Claim 6 and are rejected for the same reasons.

18. As per Claim 8, Qureshi teaches: The apparatus as claimed in claim 1, wherein at least one program instruction within said common subset of instructions performs common data processing operations in either said first mode or said second mode but generates different result data values depending upon whether said instruction decoder is operating in said first mode or said second mode (Paragraph 1, depending upon the order in which the data is presented, radically different results will result, as reading an instruction backwards will generate a very different answer as if you read it in the proper order).

Claims 19 and 30 are substantially similar to Claim 8 and are rejected for the same reasons.

19. As per Claim 9, Qureshi teaches: The apparatus as claimed in claim 8, wherein said at least one program instruction generating different result data values includes a program counter value as an input operand (Paragraph 1, if the machine is reading data in an order it wasn't intended to be read in, everything will generate different results).

Claims 20 and 31 are substantially similar to Claim 9 and are rejected for the same reasons.

20. As per Claim 10, Qureshi teaches: The apparatus as claimed in claim 9, wherein a different relationship is maintained between said program counter value and an address of an instruction being executed depending upon whether said instruction decoder is operating in said first mode or said second mode (Paragraph 1, if the machine is reading data in an order it wasn't intended to be read in, then the program counter will point to the wrong address).

Claims 21 and 32 are substantially similar to Claim 10 and are rejected for the same reasons.

21. As per Claim 11, Qureshi teaches: The apparatus as claimed in claim 8, wherein said at least one program instruction generating different result data values includes a program status register value as an input operand (Paragraph 1, if the machine is

reading data in an order it wasn't intended to be read in, everything will generate different results).

Claims 22 and 33 are substantially similar to Claim 11 and are rejected for the same reasons.

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. Claims 7, 18, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Qureshi, in view of McFarland et al. (USPN 5,781,753, herein McFarland).

24. As per Claim 7, Qureshi teaches an The apparatus as claimed in claim 1, but fails to explicitly teach:

wherein said second instruction set is a variable length instruction set.

Qureshi teaches a system to allow a first and second instruction set to run on the same processor, but does not explicitly teach that the second instruction set is a variable length instruction set. However, McFarland teaches that the x86 architecture, one of the most widely used architectures in PC's, and what made PCs into a mass-market item (Column 2, Lines 9-20), contains variable-length instructions that need to be dealt with when designing a machine to run the architecture (Column 5, Lines 56-

65). Given the popularity and wide usage of the x86 processor, and the advantage of using Qureshi's system to allow instruction sets of different formats to function together, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Qureshi's invention into a machine running an x86 architecture, which would make variable-length instructions one of the instruction sets Qureshi deals with. Claims 18 and 29 have similar limitations and are rejected for the same reasons.

Response to Arguments

25. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

26. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

27. Chang et al. (United States Patent Application Publication 2004/0059848) teaches a device for switching the endian order in a processor.

28. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert E. Fennema whose telephone number is (571) 272-2748. The examiner can normally be reached on Monday-Friday, 8:45-6:15.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Robert E Fennema
Examiner
Art Unit 2183

RF

RICHARD L. ELLIS
PRIMARY EXAMINER